ABSTRACT OF THE DISCLOSURE

In this data processor, the semiconductor chip comprises a central processing unit, an interface controller, and a bus controller. The interface controller further includes an interface control unit, a FIFO unit, and a transfer control unit. The interface control unit outputs the data of the FIFO unit to the external side of the semiconductor chip and inputs the data inputted from the external side of the semiconductor chip to the FIFO unit. The transfer control unit performs the control to transfer the data stored in the FIFO unit by designating the transfer destination address and the control to input the data to the FIFO unit by designating the transfer source address. The control by the data transfer control device is not included in the transfer control by the transfer control device. Accordingly, the time required for the data transfer between the on-chip interface controller and the external side can be curtailed.